The opinion in support of the decision being entered today was not written for publication and is not precedent of the Board.

Paper No. 60

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte TAKASHI HOTTA, SHIGEYA TANAKA and HIDEO MAEJIMA

Appeal No. 2000-1356
Application 07/979,772

HEARD: OCTOBER 26, 2000

Before FLEMING, RUGGIERO and LALL, Administrative Patent Judges.

LALL, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the final rejection[1] of all the pending claims 38, 40 to 64, 91, 92, 120 to 146, 173, 174, and 181 to 184.

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[1] There was an amendment after the final rejection [paper no. 43] which was entered by the Examiner [paper no. 46].

The invention is related to a data processing system and method wherein the speed of execution of instructions can be increased by executing a plurality of instructions in parallel wherever possible. The unique features of the invention lie in the inclusion of a conflict detector, a cache memory, a first mask and a second mask. The conflict detector evaluates each of a plurality of instructions input to the instruction unit so as to determine conflicts within the plural instructions. When conflict is detected by the conflict detector, an indication of the conflict is stored in the cache along with the plural instructions. The conflict information is used to control the sequence of feeding the instructions to the first mask and the second mask. If a conflict is detected, then one of the instructions is executed in parallel with a NOP instruction by the first and second arithmetic operation units. If no conflict is detected, then the plural instructions are executed in parallel by the first and second arithmetic units. The invention is further illustrated by the following claim below.

38. A processor system, comprising:

means for fetching a plurality of instructions;

predecode means for predecoding said plurality of instructions fetched by said fetching means and for generating information used for determining whether said plurality of instructions can be processed in parallel;

a cache memory for storing said plurality of instructions and said information generated by said predecode means, said cache memory outputs said plurality of instructions in parallel along with said information; and

an execution unit for executing said plurality of instructions based on said information output from said cache memory along with said plurality of instructions.

The Examiner relies on the following reference:

Lee et al. (Lee) 4,722,050 Jan. 26, 1988

Claims 38, 40 to 64, 91, 92, 120 to 146, 173, 174, and 181 to 184 stand rejected under 35 U.S.C. § 103 over Lee.

Rather than repeat the positions and the arguments of Appellants or the Examiner, we make reference to the briefs[2] and the answer for their respective positions.

OPINION

We have considered the rejection advanced by the Examiner. We have, likewise, reviewed Appellants' arguments against the rejection as set forth in the briefs.

[2] A reply brief was filed as paper no. 50 and was entered in the record without any response from the Examiner.

We affirm-in-part.

In rejecting a claim under 35 U.S.C. § 103, an examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to

the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We are further guided by the precedence of our reviewing court that the limitations from the disclosure are not to be imported into the claims. In re Lundberg, 244 F.2d 543, 113 USPQ 530 (CCPA 1957); In re Queener, 796 F.2d 461, 230 USPQ 438 (Fed. Cir. 1986). We also note that the arguments not made separately for any individual claim or claims are

considered waived. See 37 CFR § 1. 192 (a) and (c). In re Baxter Travenol Labs., 952 F.2d 388, 391, 21 USPQ 2d 1281, 1285 (Fed. Cir. 1991) ("It is not the function of this court to examine the claims in greater detail than argued by an appellant, looking for nonobvious distinctions over the prior art."); In re Wiechert, 370 F.2d 927, 936, 152 USPQ 247, 254 (CCPA 1967) ("This court has uniformly followed the

sound rule that an issue raised below which is not argued in this court, even if it has been properly brought here by reason of appeal is regarded as abandoned and will not be considered. It is our function as a court to decide disputed issues, not to create them.")

Analysis

At the outset, we note that the claims do not stand or fall together. We treat below the various claims under rejection and the corresponding Appellants' arguments.

Claim 38

Appellants argue [brief, page 16] that "there is no teaching or suggestion in Lee of an execution unit which executes the

instructions based on the conflict information." This argument is not commensurate with the scope of claim 38. Claim 38 does not recite the execution of instructions based on the conflict information. On the other hand, we agree with the Examiner [answer, page 7] that "the last paragraph [of claim 38] does not mention anything about parallel execution. It only says 'based on [said] information.' This may be that ... it will be executed in a pipelined manner ... based on the information output from

the cache." We find that the Examiner's position is consistent with the meaning of pipeline processing as defined by the Computer Dictionary, third edition, Microsoft Press, which states that "pipeline processing" is "[a] method of processing on a computer that allows fast parallel processing of data." Therefore, we sustain the obviousness rejection of claim 38 over Lee.

Regarding claim 40, in Lee, the information stored in cache 112 is clearly used to control the sequence of instructions flowing to the processor 116. Therefore, we

sustain the obviousness rejection of claim 40 over Lee.

With respect to claim 42, Appellants merely make a conclusory statement. Regardless, it is implicit in Lee that a branch instruction while being predecoded and fed to the processor must have associated with it information which is capable of avoiding potential conflicts among the various registers. Thus, we sustain the obviousness rejection of claim 42 over Lee.

Regarding claim 43, Appellants offer no argument other than a mere conclusory statement. For the same rationale as claim 42, we sustain the obviousness rejection of claim 43.

Regarding claim 44, Appellants merely offer a conclusory statement. As we noted above, while decoding and processing a branch instruction, Lee must resolve the resource conflict as the branch relates to the other instructions. Thus, we sustain the obviousness rejection of claim 44 over Lee.

With respect to claim 45, Appellants merely make a conclusory statement. Nevertheless, Lee’s branch instruction could include a load instruction. Therefore, we sustain the

obviousness rejection of claim 45 over Lee.

Regarding claim 46, Appellants offer a mere conclusory statement. Anyway, we find that the branch instruction in Lee could obviously involve the resolution of a conflict regarding the use of the same shifter while different kinds of branch instructions are being processed. Therefore, we sustain the obviousness rejection of claim 46 over Lee.

Regarding claim 47, Appellants offer no specific analysis other than a mere conclusory statement. At any rate, we find that when a decision is made such as the one shown by step H2 in fig. 6 of Lee, an artisan would have employed a single bit as a flag to denote the result of the decision. Consequently, we sustain the obviousness rejection of claim 47 over Lee.

With respect to dependent claim 181, an artisan would have found it obvious to introduce additional arithmetic logic units to Lee's processor to facilitate the processing of instructions. Therefore, we sustain the obviousness rejection of claim 181 over Lee.

Claim 48

Appellants argue [brief, page 18] that "[a]s shown above,

[t]here is no teaching ... in Lee regarding ... the parallel processing of the instructions when the information indicates that the instruction[s] can be processed in parallel without conflict." We are persuaded by the Examiner's position [answer, pages 7 to 10] that the information in cache 112 of Lee includes the information resulting from the resolution of the potential conflict in the processing of a branch instruction, and this information is outputted at 122A and 122B in a parallel manner to processor 116. Therefore, we sustain the obviousness rejection of claim 48 over Lee.

With respect to the dependent claims 49, 50, 51, 52, 53 and 55 (keeping in mind that the phrase "a predetermined number of bits" corresponds to the phrase "a single bit"), they

respectively include the limitations corresponding to the limitations included in the dependent claims 42, 43, 44, 45, 46 and 47 which have been discussed above. Therefore, for the rationale of claim 48 and the noted respective dependent claims, we sustain the obviousness rejection of claims 49, 50,

51, 52, 53 and 55.

Regarding the dependent claim 54, this corresponds to dependent claim 40 since an artisan would recognize that the phrase “to control the execution sequence of ... instructions” (claim 40) is equivalent to the phrase “controlling the timing of execution of ... instructions” (claim 54). Therefore, we sustain the obviousness of rejection of claim 54 for the same rational as for claim 48 and claim 40.

Claim 56

Contrary to Appellants’ arguments [brief, pages 20 and reply brief 2 to 6], Lee shows first storage means as main memory 14 and second storage means as cache 112 (fig. 3). In other respects, the above discussion regarding claim 38 equally applies here. Consequently, we sustain the obviousness rejection of claims 56 and 57 over Lee.

With respect to dependent claims 58, 59, 60, 61, 62, and 63, they respectively include limitations corresponding to those in dependent claims 41, 42, 43, 44, 45 and 46. Therefore, for the same rationale as claim 56 and the noted

dependent claims, we sustain the obviousness rejection of the dependent claims 58, 59, 60, 61, 62, and 63 over Lee.

Regarding dependent claim 64, the claimed decode means between the first and the second storage means is shown as 230 (fig. 4, and answer, page 7) by Lee. Therefore, we sustain the obviousness rejection of claim 64 over Lee.

Claim 91

Contrary to Appellants' arguments [brief, pages 22 and 23], we are persuaded by Examiner's position [answer, pages 3 to 7] that in Lee, cache memory 112 does output the claimed "at least two instructions from said plurality of instructions in the same cycle along with said information." See fig. 7, where two instructions are outputted by the cache memory in one cycle. In other respects, the discussion of claim 38 equally applies here. Consequently, we sustain the obviousness rejection of claim 91 over Lee.

With respect to its dependent claim 182, despite Appellants' arguments [brief, pages 32 to 33], an artisan would have found

it obvious to employ additional arithmetic logic units to the processor of Lee to enhance the processing speed. Therefore, we sustain the obviousness rejection of claim 182 over Lee.

Claim 92

Claim 92 further adds to claim 91 the limitation of "parallel processing said at least two instructions ... without conflict." This limitation was discussed in regard to claim 48 above. Therefore, for the same rationale as claim 91 and claim 48, we sustain the obviousness rejection of claim 92 over Lee.

Independent claims 120, 130, 138, 173 and 174, and their dependent claims

These independent claims each contains a limitation equal to, or similar to, the limitation of "a state of said plurality of instructions and information remaining in said cache memory after output of said plurality of instructions is the same as the state of said plurality of instructions and information before output of said plurality of instructions" (claim 120). We do not find, and neither has the Examiner specifically identified, any discussion in Lee regarding the above limitation. Therefore, we

do not sustain the obviousness rejection over Lee of independent claims 120, 130, 138, 173 and 174, and their dependent claims 121 through 129 and 183, 131 through 137, 139 through 146, and 184.

In summary, we have sustained the obviousness rejection over Lee of claims 38, 40 to 64, 91, 92, 181 and 182, but not of claims 120 to 146, 173, 174, 183 and 184.

Accordingly, the decision of the Examiner rejecting claims 38, 40 to 64, 91, 92, 120 to 146, 173, 174, and 181 to 184 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

MICHAEL R. FLEMING Administrative Patent Judge	)	
JOSEPH F. RUGGIERO Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES

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